

## CLAIMS

What is claimed is:

- 1    1.     A method comprising:  
2           performing a first memory access procedure, in response to receiving a first  
3    memory access procedure command over a command bus, wherein the first memory  
4    access procedure causes a memory module to perform multiple accesses of first  
5    memory locations associated with the memory module, and the first memory access  
6    procedure is selected from a group of procedures that includes a memory  
7    initialization procedure and a memory test procedure.
  
- 1    2.     The method of claim 1, further comprising:  
2           sending, over the command bus, a status message, which indicates that the  
3    memory module has completed the first memory access procedure.
  
- 1    3.     The method of claim 1, further comprising:  
2           receiving a second memory access procedure command over the command  
3    bus; and  
4           performing a second memory access procedure, in response to the second  
5    memory access procedure command, wherein the second memory access procedure  
6    causes the memory module to perform multiple accesses of the first memory  
7    locations associated with the memory module, and the second memory access  
8    procedure is the memory test procedure.
  
- 1    4.     The method of claim 3, further comprising:  
2           sending, over the command bus, a status message, which indicates that the  
3    memory module has completed the memory test procedure.
  
- 1    5.     A method comprising:  
2           receiving an initialization command over a command bus; and

3 performing an initialization procedure, in response to the initialization  
4 command, during which a memory module initializes one or more memory storage  
5 units by generating and sending data packets with initialization data to the one or  
6 more memory storage units.

1 6. The method of claim 5, further comprising:  
2 sending, over the command bus, a status message, which indicates that the  
3 memory module has completed the initialization procedure.

1 7. The method of claim 5, further comprising:  
2 performing a testing procedure, during which the memory module tests the  
3 one or more memory storage units by reading data within memory locations of the  
4 one or more memory storage units, and comparing the data with the initialization  
5 data.

1 8. A method comprising:  
2 receiving a test command over a command bus; and  
3 performing a testing procedure, in response to the test command, during  
4 which a memory module tests one or more memory storage units by reading data  
5 within memory locations of the one or more memory storage units, and comparing  
6 the data with expected data.

1 9. The method of claim 8, further comprising:  
2 sending, over the command bus, a status message, which indicates that the  
3 memory module has completed the testing procedure.

1 10. The method of claim 8, further comprising:  
2 sending, over the command bus, error information, which indicates that the  
3 memory module has encountered at least one error during the testing procedure.

1 11. The method of claim 8, further comprising:  
2 performing an initialization procedure, before performing the testing  
3 procedure, during which the memory module initializes the one or more memory  
4 storage units by writing initialization data to the memory locations of the one or  
5 more memory storage units.

1 12. A method comprising:  
2 a first memory module performing a first memory access procedure, which  
3 causes the first memory module to perform multiple accesses of first memory  
4 locations associated with the memory module, wherein the first memory access  
5 procedure is selected from a group of procedures that includes a memory  
6 initialization procedure and a memory test procedure; and  
7 at least one additional memory module performing a second memory access  
8 procedure, which causes the at least one additional memory module to perform  
9 multiple accesses of second memory locations associated with the at least one  
10 additional memory module, wherein the first memory access procedure and the  
11 second memory access procedure include substantially similar process steps, and  
12 wherein at least a portion of the first memory access procedure is performed in  
13 parallel with at least a portion of the second memory access procedure.

1 13. The method of claim 12, wherein the first memory access procedure and the  
2 second memory access procedure include memory initialization procedures  
3 performed during an initialization of a computer system.

1 14. The method of claim 12, further comprising:  
2 the first memory module performing a third memory access procedure,  
3 which causes the first memory module to perform multiple additional accesses of  
4 the first memory locations associated with the memory module, wherein the third  
5 memory access procedure is a memory test procedure; and

6           the at least one additional memory module performing a fourth memory  
7   access procedure, which causes the at least one additional memory module to  
8   perform multiple additional accesses of the second memory locations associated  
9   with the at least one additional memory module, wherein the fourth memory access  
10   procedure is the memory test procedure, and wherein at least a portion of the fourth  
11   memory access procedure is performed in parallel with the third memory access  
12   procedure.

1   15.    The method of claim 14, wherein the third memory access procedure and the  
2   fourth memory access procedure include memory test procedures performed during  
3   an initialization of a computer system.

1   16.    A method comprising:  
2           a first memory module performing a first initialization procedure of first  
3   memory locations associated with the first memory module; and  
4           at least one additional memory module performing at least one additional  
5   initialization procedure of second memory locations associated with the at least one  
6   additional memory module, wherein at least a portion of the first initialization  
7   procedure is performed in parallel with at least a portion of the at least one  
8   additional initialization procedure.

1   17.    The method of claim 16, further comprising:  
2           the first memory module receiving a module initialization command; and  
3           the first memory module initiating the first initialization procedure in  
4   response to receiving the command.

1   18.    The method of claim 17, further comprising:  
2           a processor generating and sending the module initialization command.

- 1     19.     The method of claim 16, wherein performing the first initialization  
2     procedure comprises:  
3             the first memory module generating and sending data packets to the first  
4     memory locations, wherein the data packets include initialization data.
- 1     20.     The method of claim 16, further comprising:  
2             the first memory module performing a first test procedure of the first  
3     memory locations; and  
4             the at least one additional memory module performing at least one additional  
5     test procedure of the second memory locations, wherein at least a portion of the first  
6     test procedure is performed in parallel with at least a portion of the at least one  
7     additional test procedure.
- 1     21.     A method comprising:  
2             generating and sending multiple memory initialization commands to  
3     multiple memory modules of a memory subsystem;  
4             the multiple memory modules receiving the multiple memory initialization  
5     commands; and  
6             selected ones of the multiple memory modules performing an initialization  
7     procedure in parallel, in response to receiving an initialization command.
- 1     22.     The method of claim 21, wherein performing the initialization procedure  
2     comprises:  
3             the selected ones of the multiple memory modules generating and sending  
4     data packets to memory locations located logically behind the multiple memory  
5     modules, wherein the data packets include initialization data.
- 1     23.     The method of claim 21, further comprising:

2 polling the selected ones of the multiple memory modules to determine  
3 when the selected ones of the memory modules have completed the initialization  
4 procedure.

1 24. The method of claim 21, further comprising:  
2 a processor generating and sending multiple memory test commands to the  
3 multiple memory modules;  
4 the multiple memory modules receiving the multiple memory test  
5 commands; and  
6 selected ones of the multiple memory modules performing a test procedure  
7 in parallel, in response to receiving a test command.

1 25. The method of claim 24, further comprising:  
2 polling each of the multiple memory modules to determine when each of the  
3 memory modules has completed the test procedure.

1 26. A buffer module comprising:  
2 a bus interface, which is connectable to a command bus;  
3 a controller, which, in response to the buffer module receiving an  
4 initialization command over the command bus, is operable to perform an  
5 initialization procedure, which includes initializing one or more memory storage  
6 units by generating and sending data packets with initialization data to the one or  
7 more memory storage units; and  
8 a storage unit interface, which is connectable to a storage unit link, and  
9 which enables the buffer module to communicate with the one or more memory  
10 storage units.

1 27. The buffer module of claim 26, wherein the controller is further operable to  
2 send, over the command bus, a status message, which indicates that the buffer  
3 module has completed the initialization procedure.

1 28. The buffer module of claim 27, wherein the controller is further operable to  
2 perform a testing procedure, which includes testing the one or more memory storage  
3 units by reading data within memory locations of the one or more memory storage  
4 units, and comparing the data with the initialization data.

1 29. The buffer module of claim 28, wherein the controller is further operable to:  
2 receive a test command over the command bus; and  
3 perform the testing procedure in response to receiving the test command.

1 30. The buffer module of claim 28, wherein the controller is further operable to  
2 send, over the command bus, a status message, which indicates that the buffer  
3 module has completed the testing procedure.

1 31. The buffer module of claim 28, wherein the controller is further operable to  
2 send, over the command bus, error information, which indicates that the buffer  
3 module has encountered at least one error during the testing procedure.

1 32. A memory module comprising:  
2 one or more memory storage units; and  
3 a buffer module, which includes  
4 a bus interface, which is connectable to a command bus,  
5 a controller, which, in response to the buffer module receiving an  
6 initialization command over the command bus, is operable to  
7 perform an initialization procedure, which includes initializing one or  
8 more memory storage units by generating and sending data packets  
9 with initialization data to the one or more memory storage units, and  
10 a storage unit interface, which is connectable to a storage unit link, and  
11 which enables the buffer module to communicate with the one or  
12 more memory storage units.

1 33. The memory module of claim 32, wherein the controller is further operable  
2 to perform a testing procedure, which includes testing the one or more memory  
3 storage units by reading data within memory locations of the one or more memory  
4 storage units, and comparing the data with the initialization data.

1 34. The memory module of claim 32, wherein the one or more memory storage  
2 units and the buffer module form a portion of a dual in-line memory module.

1 35. The memory module of claim 32, wherein the one or more memory storage  
2 units include one or more dynamic random access memory components.

1 36. An electronic system comprising:  
2 a memory controller; and  
3 multiple memory modules, operatively coupled to the memory controller,  
4 wherein each memory module includes  
5 one or more memory storage units, and  
6 a buffer module, which includes  
7 a bus interface, which is connectable to a command bus,  
8 a memory module controller, which, in response to the buffer module  
9 receiving an initialization command over the command bus, is  
10 operable to perform an initialization procedure, which includes  
11 initializing one or more memory storage units by generating and  
12 sending data packets with initialization data to the one or more  
13 memory storage units, and  
14 a storage unit interface, which is connectable to a storage unit link, and  
15 which enables the buffer module to communicate with the one or  
16 more memory storage units.

1 37. The electronic system of claim 36, further comprising:



2 a processor, which is operable to initiate the initialization procedure by  
3 sending multiple module initialization messages to the multiple memory modules.

1 38. The electronic system of claim 36, wherein the memory controller is further  
2 operable to initiate the initialization procedure by sending multiple module  
3 initialization messages to the multiple memory modules.

1 39. The electronic system of claim 36, wherein the memory module controller is  
2 further operable to perform a testing procedure, which includes testing the one or  
3 more memory storage units by reading data within memory locations of the one or  
4 more memory storage units, and comparing the data with the initialization data.

1 40. The electronic system of claim 39, further comprising:  
2 a processor, which is operable to initiate the testing procedure by sending  
3 multiple module test messages to the multiple memory modules.

1 41. The electronic system of claim 39, wherein the memory controller is further  
2 operable to initiate the testing procedure by sending multiple module test messages  
3 to the multiple memory modules.

1 42. The electronic system of claim 36, wherein at least some of the multiple  
2 memory modules include dual in-line memory modules.

1 43. The electronic system of claim 36, wherein the one or more memory storage  
2 units include one or more dynamic random access memory components.

1 44. The electronic system of claim 36, wherein at least some of the multiple  
2 memory modules are to perform at least portions of the initialization procedure in  
3 parallel with each other.

1 45. The electronic system of claim 36, wherein the electronic system includes a  
2 computer.

1 46. An apparatus comprising:  
2 means for receiving an initialization command over a command bus;  
3 means for performing an initialization procedure, in response to the  
4 initialization command, which enables the apparatus to initialize one or more  
5 memory storage units by generating and sending data packets with initialization data  
6 to the one or more memory storage units; and  
7 means for communicating with the one or more memory storage units.

1 47. The apparatus of claim 46, further comprising:  
2 means for sending a status message over the command bus, which enables  
3 the apparatus to indicate that the apparatus has completed the initialization  
4 procedure.

1 48. The apparatus of claim 46, further comprising:  
2 means for performing a testing procedure, which enables the apparatus to  
3 test the one or more memory storage units by reading data within memory locations  
4 of the one or more memory storage units, and comparing the data with the  
5 initialization data.

1 49. The apparatus of claim 48, further comprising:  
2 means for sending a status message over the command bus, which enables  
3 the apparatus to indicate that the apparatus has completed the testing procedure.

1 50. The apparatus of claim 48, further comprising:  
2 means for sending error information over the command bus, which enables  
3 the apparatus to indicate that the apparatus has encountered at least one error during  
4 the testing procedure.